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The block diagram illustrates the control system architecture. It features several interconnected components:

- Input Section:** Includes an "入力回路" (Input Circuit) connected to "入力端子" (Input Terminals), which feeds into a "比較器" (Comparator).
- Control Logic:** A central logic unit containing a "AND" gate, an "OR" gate, and a "NOT" gate, along with various signal lines labeled "A", "B", "C", "D", "E", "F", "G", "H", "I", "J", "K", "L", "M", "N", "O", "P", "Q", "R", "S", "T", "U", "V", "W", "X", "Y", "Z".
- Output Section:** The logic unit controls two output relays: "出力用リレー" (Output Relay) and "停止用リレー" (Stop Relay). These are connected to "出力端子" (Output Terminals) and "停止端子" (Stop Terminals).
- Power Supply:** A "電源" (Power Source) provides power to the system via a "電源線" (Power Line).
- Feedback Loop:** An "出力監視回路" (Output Monitoring Circuit) monitors the output and provides feedback to the input circuit.
- Interlocks:** Various interlocking mechanisms are shown, such as "出力監視回路" (Output Monitoring Circuit) and "出力監視回路" (Output Monitoring Circuit).

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PATENT FAMILY SEARCH FOR JP 02-237220

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SOURCES:

Selected file: PLUSPAT

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Selected file: WPAT

Derwent World Patents Index, (c) Thomson Scientific
UP (basic), UE(equiv), UA (poly), UB (chem) : updates through 2006-12
Manual Code Revision 2006 - final lists available on Thomson Scientific
Website. Revised codes will be implemented in the first update of 2006.
Please review lists to update manual codes in SDIs and stored searches.
Last database update : 2006/02/18 (YYYY/MM/DD)

Selected file: INPD

INPADOC International Patent Documentation Center
Source: European Patent Office - EPIDOS
Individual publication stage records for each Patenting Authority
Coverage: 75 patent offices ; start dates vary from 1968 forward
Current through weekly update 2006-07/up ; last update 2006/02/17
IPC Classes: for searching prior to 2006, use the qualifier: /IC
For searching IPC v8 (pd>=2006), use the qualifiers: /ICAA /ICCA

Selected file: USPAT

US Patents Full Text of United States Patent and Trademark Office
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Selected file: USAPPS

US Patent Applications full-text from USPTO (c) Questel.Orbit
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Std Biblio thru PGP PD=2001-11(2002-11/uam); Grant PD=2005-06(2006-02/UM)
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From 06/04 forward questionable source data received from USPTO shows
PCT filing date, not date of national stage as app date for US patents
that entered via PCT route. IFI is investigating.

PATOLIS-e

PATENT FAMILY

#	Patent No.	Kind	Date	Applic.No.	Date
1)	JP02237220	A	19900919	1989JP-0056942	19890309

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1 / 1 PLUSPAT - ©QUESTEL-ORBIT - image
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 Patent Assignee :
 (A) FUJITSU LTD
 Patent Assignee :
 (A) FUJITSU LTD
 Inventor(s) :
 (A) HIROCHI KATSUJI
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 Inventor: HIROCHI KATSUJI
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 Title of Invention: OUTPUT CIRCUIT

Abstract: PURPOSE: To set the fall change of an output signal to be gradual
 1 and to evade the ringing of the waveform of an output fall by increasing a
 base current supplied to an L level driving means stepwise. CONSTITUTION: W
 hen the output of an input circuit changes from a first potential state to a
 second potential state, a first base current ia is firstly generated, the L
 level driving means is operated by the first base current ia and the potent
 ial of an output terminal is changed from an H level to an L level. When the
 potential of the output terminal reaches a prescribed potential, second bas
 e currents il-in are generated and they are added to the first base current
 ia. Since the base current IB is added with the lapse of time so as to incre
 ase them stepwise, the fall change of the output signal comes to gradual and
 the occurrence of the ringing of the output fall waveform can be evaded. COP
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 (A7D2 1992/ 9/28, NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE),
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 (A7D2 1993/ 8/20, NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE),
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